REMARKS

The present communication is responsive to the Official Action mailed January 3, 2006. A petition for a three-month extension of the term for response, to and including July 3, 2006, is transmitted herewith.

Claim 20 and other claims dependent thereon, were rejected under 35 U.S.C. § 102 as anticipated by *Salatino et al.*, U.S. Patent No. 5,915,168 ("*Salatino* '168"). By the present amendment, claim 20 has been modified to clarify its language and to more clearly state that which was in claim 20 as previously presented. The recitation of "at least one wafer-level transparent packaging layer" has been changed to -- a wafer-level transparent packaging layer -- so that there can be no doubt as to which layer is referred to. In this regard, claim 20 is an "open" claim (note the transition "comprising"), and thus the recitation of providing "a" wafer-level transparent packaging layer does not exclude the possibility of providing additional wafer-level transparent packaging layers not referred to in the claim. Also, the claim has been amended to positively recite that the step of forming the "wafer-level spacer" includes applying a "spacer material separate from the wafer-level transparent packaging layer" to that layer. One example of a process in which a "spacer material" is applied is shown in FIG. 4B of the drawings, and discussed at paragraph 51 of the specification.[1] The sealing step has been modified to more clearly refer to sealing the wafer-level spacer to the "wafer" referred to in the claim, and to refer to the "cavities" that are mentioned in the preceding "forming" step rather than to a "gap." The "dicing" step has been amended to expressly note that the devices formed by such

[1] Paragraph numbers herein refer to the published specification (U.S. 2002/0027296A1.

step must include a microstructure, a portion of the packaging layer, and a cavity disposed between the microstructure and such portion of the packaging layer. The recitation concerning "without removing material of the wafer-level transparent packaging layer" has been moved to the end of the claim and clarified. Merely by way of example, the entire sequence of process steps shown in FIGS. 4A-5I inclusive is performed without removal of material from the wafer-level transparent packaging layer 300, 400.

It is respectfully submitted that claim 20 as amended distinguishes over *Salatino* '168. The Official Action characterizes element 236 depicted in, *e.g.*, FIGS. 2 and 3 of the reference, as the "spacer." The Official Action, however, also relies on the "glass or quartz cover wafer" disclosed at column 4, line 66 of the reference as constituting the "at least one transparent chip scale packaging layer." It is respectfully submitted that this interpretation of *Salatino* '168 cannot properly support a § 102 anticipation rejection, inasmuch as it combines features from two very different embodiments shown in the reference. Stated another way, *Salatino* '168 does not expressly or implicitly suggest that the "cover wafer layer 401" shown in FIG. 9 (the glass or quartz wafer) could be or should be used in conjunction with the asserted spacer 236 as contemplated in the Official Action. Modification of the reference teachings, to combine features of different embodiments, would be necessary, even according to the rationale of the Official Action, to meet the features of claim 20. For that reason alone, *Salatino* '168 cannot support a § 102 rejection of claim 20.

Moreover, even assuming for purposes of argument that one could combine the features of disparate embodiments in the reference, *Salatino* '168 still would not meet the features of claim 20. The step of forming spacer 236 manifestly does not

meet the "forming" recitation of claim 20 inasmuch as the asserted spacer 236 is formed on the wafer, *i.e.*, element 200, and not on a wafer-level packaging layer of any type, much less a transparent packaging layer, as now recited in claim 20.

Salatino '168 additionally fails to anticipate claim 20, because, in each and every process taught by the reference, portions of the lid wafer clearly are removed prior to dicing. For example, in the process of FIGS. 2-4, "the silicon layer 261 of the lid wafer 260 is removed and insulating layer 262 is thinned by etching or lapping to expose openings 248 and contact pads 250" (col.3 ll.50-53), whereas in the process of FIGS. 5-6, the n+ silicon portion 280 of the lid wafer is removed by "using a KOH etch" so as to expose openings 248 and contacts 250 (col.4 ll.6-10). In the process of FIGS. 9-11, "the cover wafer is partially removed by etching or lapping" so as to expose the "scribe cavities," and after such removal, "the individual dies can then be separated." (Col.5 ll.19-22.)

In this regard, the Examiner's comments to the effect that the "gaps" formerly recited could be formed "without requiring removal of material from said at least one transparent packaging layer" (Official Action at 3) are noted. To the extent that these comments would apply to the claim as formerly presented, they clearly do not apply to the claim as now presented. Thus, even if it is assumed that *Salatino* '168's layer 401 (FIG. 9) is initially formed with cavities 406 "rather than formed as a planar layer and then patterned to form the cavities" as asserted in the Official Action, the *Salatino* '168 process as a whole still requires removal of material from the layer prior to the dicing step.

For all of these reasons, the 35 U.S.C. § 102 rejection of claim 20 on *Salatino* '168 should be withdrawn.

The § 102 rejection on *Salatino* '168 should also be withdrawn as to claims 22-23 and 40-42 inclusive, inasmuch as each of these claims depends from claim 20. Claims 27-28, 34, 39, 44-45, and 48, also encompassed by this rejection, have been canceled by the present amendment. Each of claims 22, 40, and 42 has been amended for consistency with amended claim 20. The absence of new matter is believed apparent from the amendatory matter itself.

Claims 24, 33, 36, 47, and 49-50 were rejected under 35 U.S.C.§ 103(a) as unpatentable over *Salatino* '168 further in view of *Ichikawa et al.*, U.S. Patent No. 5,996,199 ("*Ichikawa* '199"). This rejection is believed to be moot inasmuch as these claims have been canceled. Further, *Ichikawa* '199 was not asserted as teaching anything which would remedy the deficiencies of *Salatino* '168 pointed out above in connection with claim 20, but was merely cited as teaching particular materials no longer recited in the claims.

Claim 65 was rejected under 35 U.S.C. § 103(a) as unpatentable over *Salatino* '168 in view of *Chen*, U.S. Patent 6,083,766 ("*Chen* '766"). Here again, *Chen* '766 was not cited as teaching anything which would remedy the deficiencies of *Salatino* '168, but instead was merely cited as teaching plating electrical contacts onto "edge surfaces." Moreover, by the present amendment, claim 65 has been modified to more clearly point out that the step of forming electrical contacts occurs "prior to completion of the dicing step," and is performed so that the contacts extend "away from the wafer-scale transparent packaging layer." The recitation that this step is performed so that the contacts extend along "edge surfaces" has been clarified to state that the contacts extend along surfaces which constitute edge surfaces of the individual chip scale package devices "after completion of the dicing step." For example, contacts 412 (FIG. 5G) are formed prior to completion of the

dicing step and extend away from wafer-level transparent packaging layer 400. After completion of the dicing step (FIG. 5I), these contacts lie on edge surfaces of the individual chip scale devices.

New claims 68-70 have been added to further particularize some of the steps associated with formation of the contacts. These new claims are supported, *inter alia*, by FIGS. 5E-5I and the associated disclosure in the specification at paragraphs 0056-0057, as well as, *e.g.*, FIG. 2A and paragraphs 0039-0040. For example, in the specific example set forth at paragraphs 0056-0057, the "epoxy layer 408" recited in the specification constitutes the "layer material."

It is respectfully submitted that neither *Salatino* '168 nor *Ichikawa* '199 teaches the steps recited in amended claim 65 or new claims 68-70. In *Salatino* '168, the only contacts shown (250, FIGS. 2-6; 306, FIGS. 7, 8; and unnumbered in FIG. 13) clearly do not lie on edge surfaces of an individual device after dicing, and clearly are not formed so as to extend away from a wafer-level transparent packaging layer. Indeed, at the time these contacts are formed, there is no wafer-level transparent layer. In *Ichikawa* '199, the electrodes (80, 90, FIG. 5E) clearly are formed after creation of an individual device, and are not formed prior to completion of a severing step. Neither of these references teaches application of a "layer material" as recited in claim 69, or formation of notches as referred to in claim 70. In connection with claims 65 and 68-70, the Examiner's attention is respectfully directed to commonly owned WO 95/19465; U.S. Patent No. 5,455,455; U.S. Patent No. 5,547,906; and to U.S. Patent No. 6,168,965, also of record. None of these references, however, have been asserted as relevant to formation of a packaged device having a cavity as recited in claim 20, and as included in claims 65 and 68-70 by dependency.

New claim 71 refers to an "underlying packaging layer. In the specific example of paragraphs 0056-0057, the underlying packaging layer is layer 410. This new claim, along with new claim 72 – specific to use of an "epoxy" as the layer material referred to in claim 69, are believed allowable for the reasons advanced above with respect to claims 65 and 69.

New claims 73 and 74 combine with claim 20 a further significant feature, namely, that the wafer-level spacer is formed by a process which includes a selective exposure to illumination so as to pattern the spacer material and thereby form the wafer-level spacer. These claims are supported, *inter alia*, by FIGS. 4C-4D and paragraphs 0051-0052 of the specification. Nothing in any reference of record has been asserted as teaching formation of a package spacer with cavities using this technique.

New claims 75-77 are supported by, *e.g.*, FIG. 4E and 5A-5I of the specification. The array of spacer elements 306 is seen clearly in FIG. 4E. Disposition of spacer elements 306 next to one another is seen in FIG. 4D. In this specific example, the openings referred to in claim 76 are the small gaps between adjacent spacer elements. The term "opening" is used to avoid confusion with the terms "gap" and "cavity" used in other portions of the present specification. Disposition of the adhesive 402 in these openings is seen in FIGS. 5A-5E, whereas dicing of the adhesive in the openings (claim 77) is illustrated in FIGS. 5H and 5I, which also illustrate cutting in alignment with the openings (claim 76). Nothing in the art is seen as suggesting dicing of an adhesive disposed in openings between mutually adjacent spacer elements as recited in claim 77. Claim 78 specifies disposition of an array of microlenses (*e.g.*, 100, FIG. 2A) within a cavity (*e.g.*, 120, FIG. 2A). Of course, because each of the aforementioned new claims 68-78 depends directly or indirectly from claim 20, the distinctions advanced

above with respect to claim 20 are also applicable to these claims.

New independent claim 79 recites, in somewhat different terms, the placement of individual spacer elements on the chips and with openings between spacer elements disposed on adjacent chips, the use of an adhesive extending into such openings, and dicing along severance planes extending through the openings and the adhesive. These claims are supported by the same disclosures referred to above in connection with claims 75-77. Here again, nothing in the art has been pointed out as teaching severance through openings between spacer elements, which openings contain an adhesive. New claim 79 is thus believed allowable, along with claims 80 and 81, dependent thereon.

In connection with claims 76 and 79, the Examiner's attention is respectfully directed to *Kurle et al.*, U.S. Patent 6,106,735 of record. *See* FIGS. 1G, 2; col.3 ll.17 *et seq.* However, this reference clearly does not contemplate severing through an adhesive disposed in an opening.

New independent claim 82 is believed to distinguish over the art, and to be supported by the disclosure, for reasons directly analogous to those pointed out above in connection with dependent 73. Claims 83 and 84 are likewise believed allowable.

New independent claim 85 corresponds to claim 20 as amended, with the difference being that the optoelectronic device of claim 20 is specified as an optoelectronic image sensor in claim 85 and the prohibition against removal of material refers only to those portions of the wafer-level transparent packaging layer overlying the image sensor. Dependent claims 86-102 correspond to the pending claims depending on claim 20. Claims 85-102 are allowable for the same reasons as claim 20 and the pending claims depending on claim 20 as argued above. These claims are supported by the same

disclosures supporting claims 20-84 as discussed above. The image sensor element is supported by, *inter alia*, FIGS. 2A-2C and paragraphs 0039-0047 of the specification.

As it is believed that all of the rejections set forth in the Official Action have been fully met by the foregoing amendments, arguments and remarks, favorable reconsideration and allowance are earnestly solicited.

If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that he telephone applicant's attorney at (908) 654-5000 in order to overcome any additional objections which he might have.

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

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Respectfully submitted,

By_____

Marcus J. Millet
Registration No.: 28,241
LERNER, DAVID, LITTENBERG,
KRUMHOLZ & MENTLIK, LLP
600 South Avenue West
Westfield, New Jersey 07090
(908) 654-5000
Attorney for Applicant

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